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HONEYWELL/IFL
Patent Services
101 Columbia Road
P.O.Box 2245
Morristown, NJ 07962-2245

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/699,311
Filing Date: October 30, 2003
Appellant(s): FYE, JAMES C.

Arno T. Naeckel
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/27/2010 appealing from the Office action mailed 3/9/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party of interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

1-28

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US 2002/0147987	Reynolds et al.	10-2002
US 2002/0078447	Mizutome et al.	06-2002
US 6,487,719	Itoh et al.	11-2002
US 5,88,3676	Miyazaki	03-1999
US 6,118,498	Reitmeier	09-2000
US 6,456,335	Miura	09-2002

US 2002/0150248	Kovacevic	10-2002
EP 1158788	Machida et al.	11-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-5, 7-8, 11-12, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome et al. (US20020078447, hereinafter Mizutome).

Regarding claims 1, 7 and 19, Machida discloses an apparatus for display of video data (image generation apparatus 100, see Fig. 3), the apparatus comprising:

a switch network (image selection means 101, see Fig. 3) including an output (see Fig. 3) and an input (see Fig. 3), and

a plurality of video processing pipelines (image processing means 102, see Fig. 3), each video processing pipeline including an input coupled to the switch network output (see Fig. 3),

wherein the switch network is configured to connect any of the switch inputs to any of the video processing pipeline inputs (see Fig. 3).

Machida does not specifically disclose a plurality of video sources,

a plurality of video channels configured to be coupled to different video sources,

a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels and comprising:

an output,

an input coupled to one or more video channels, to receive video data from the one or more video channels, and to decode the received video data, or

a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface configured to provide an option to a user to direct the switch network to connect a specific video decoder output to a particular view window of the apparatus for display.

In an analogous art, Reynolds discloses a plurality of video sources (see Fig. 1),

a plurality of video channels configured to be coupled to different video sources (see Fig. 1),

a plurality of video decoders (video decoders 220/224/228, see Fig. 2) coupled to the plurality of video channels (see Fig. 2), each video decoder coupled to a different one of the plurality of video channels (see Fig. 2) and comprising:

an output (see Fig. 2), and

an input coupled to one or more video channels (see Fig. 2), to receive video data from the one or more video channels (see Figs. 1-2), and to decode the received video data (see Fig. 2).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Machida's system to include the limitations as taught by Reynolds for the advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images.

Machida in view of Reynolds does not specifically disclose a manual I/O interface in operable communication with the plurality of video processing pipelines, the manual I/O interface configured to provide an option to a user to direct the switch network to connect a specific video decoder output to a particular view window of the apparatus for display.

In an analogous art, a manual I/O interface (user interface 124/remote controller 125, see Mizutome, Figs. 1 and 2) in operable communication with a plurality of video processing pipelines (see Mizutome, Fig. 1), the manual I/O interface (user interface 124/remote controller 125, see Mizutome, Figs. 1 and 2) configured to provide an option to a user to direct a network to connect a specific video decoder output to a particular view window of an apparatus for display (Mizutome discloses that a user may use the remote control to choose from various screen layout selections in which various input sources may be viewed in different windows, positions, etc. {see Mizutome, [0082], lines 1-8, [0104], lines 1-6 and Fig. 4}, and also that a user may alter a screen layout into a suitable format for viewing and listening, i.e., alter the screen layout so that a particular source is view in a specific window{see Mizutome, [0105], lines 1-5 and Fig. 4 and Fig. 20}).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds to include the limitations as taught by Mizutome for the advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images in an output mode preferred by a user (see Mizutome, [0013]).

Regarding claim 4, Machida in view of Reynolds and Mizutome discloses a plurality of video processing pipelines (image processing means 102, see Machida, Fig. 3) configured to process decoded video data (the decoded video data of Reynolds, see Fig. 2, corresponds to the image inputs of Machida) of a plurality of video sources (see Reynolds, Fig. 1) received from a plurality of video decoders (see Reynolds, Fig. 2).

Regarding claims 5, 8 and 22, Machida in view of Reynolds and Mizutome discloses a greater number of video decoders than video processing pipelines (Machida discloses that the images selected to be output may be less than the images input, and therefore the plurality of video processing means are respective to the images selected to be output, see Machida, col 5, lines 28-41 and Fig. 3; since the image inputs of Machida correspond to the video decoder outputs of Reynolds, Machida in view of Reynolds reasonably teaches a greater number of video decoders than video processing pipelines) and wherein the apparatus further comprises a display/control logic (screen control means 106, see Machida, Fig. 3) configured to control a process order of the video data from the plurality of video sources (see Machida, col 5, lines 17-19).

Regarding claim 11, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality

of video decoders, a frame in the video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2).

Regarding claim 12, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, a field of a frame in the video data (since an entire video signal is decoded, a frame of video is therefore decoded, and therefore a field of a frame is decoded, see Reynolds, Fig. 2).

3. Claims 2-3 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claims 1 and 19 above, and further in view of Itoh (of record).

Regarding claims 2 and 20, Machida in view of Reynolds and Mizutome discloses an image size/location logic (image selection means 101/adapted image synthesization means 105/screen control means 106, see Machida, Fig. 3) coupled between the manual I/O interface (as the manual I/O interface of Mizutome is connected to the system via a CPU bus, which would reasonably correspond to the screen control means 106 of Machida, it is reasonably taught that the image size/location logic is coupled between the manual I/O interface, see Mizutome Fig. 1 and Machida, Fig. 3) and each video processing pipeline output (see Machida, Fig. 3), the image size/location logic configured to receive a signal indicating designated size of a display window (display window size must be designated since the sizes of the images are designated in proportion to the screen size, see Machida, col 5, lines 17-27), the image size/location logic

further configured to determine a location in the display window (see Machida, col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for display for the video data (see Machida, col 5, lines 17-23) for each of the plurality of video sources (see Reynolds, Fig. 2) including video data for display (see Machida, col 5, lines 17-23).

Machida in view of Reynolds and Mizutome does not specifically disclose an indication of which of a plurality of video sources includes video data for display in a display window.

In an analogous art, Itoh discloses an indication of which of a plurality of video sources includes video data for display in a display window (see col 12, lines 53-60).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Itoh, for the advantage of conserving the processing resources of the system by only providing only the necessary processing for specific signals.

Regarding claims 3 and 21, Machida in view of Reynolds and Mizutome, and further in view of Itoh discloses a plurality of scalers (image processing means 102, see Machida, Fig. 3) coupled to a plurality of video decoders (see Dawson, Fig. 1A) and a plurality of video processing pipelines (see Machida, Fig. 3), wherein the plurality of scalers are each configured to scale decoded video data from the plurality of video sources (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

4. Claims 6, 9-10 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claims 1 and 7 above, and further in view of Miyazaki (of record).

Regarding claims 6 and 27, Machida in view of Reynolds and Mizutome discloses a plurality of video processing pipelines, a plurality of video sources and processed decoded data, but does not specifically discloses a memory device, or a write multiplexer coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device.

In an analogous art, Miyazaki discloses a memory device (VRAM 18A, see Fig. 1), and a write multiplexer (mux 12, see Fig. 1) coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device (see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Miyazaki for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 9, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses storing a processed decoded portion of video data into a portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 10, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display (see Miyazaki, col 7, lines 44-67 and col

8, lines 1-14), upon determining (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14) that the plurality of video processing pipelines (see Machida, Fig. 3) has completed processing the decoded portion of the video data (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 28, Machida in view of Reynolds and Mizutome, and further in view of Miyazaki discloses a clock multiplier network (see Miyazaki, col 13, line 35), the clock multiplier network controlling a rate of operation of the write multiplexer (see Miyazaki, col 13, lines 35-37).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 7 above, and further in view of Reitmeier (of record).

Regarding claim 13, Machida in view of Reynolds and Mizutome discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, but does not specifically disclose decoding a scaled field of a frame in the video data.

In an analogous art, Reitmeier discloses decoding a scaled field of a frame in the video data (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Reitmeier for the advantage of conserving memory resources.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record), Reitmeier (of record), Miyazaki (of record) and Mizutome (previously cited).

Regarding claim 14, Machida discloses a method for displaying video data, comprising:

inputting an image into a first video processing pipeline (image processing means 102, see Fig. 3) via a non-blocking switch network (image selection means 101, see Fig. 3);

inputting a second image into a second video processing pipeline (image processing means 102, see Fig. 3) via the non-blocking switch network (image selection means 101, see Fig. 3);

processing, by the first video processing pipeline the first image (see Fig. 3);

processing, by the second video processing pipeline the second image (see Fig. 3).

Machida does not specifically disclose receiving a first video data from a first video source at a first video decoder via a first video channel;

receiving a second video data from a second video source at a second video decoder via a second video channel;

decoding, via the first video decoder, a first frame of the first video data;

decoding, via the second video decoder, a second frame of the second video data;

inputting the first decoded frame into an image into a first video processing pipeline via a non-blocking switch network;

inputting the second decoded frame into a second image into a second video processing pipeline via the non-blocking switch network;

processing, by the first video processing pipeline the first image decoded frame;

processing, by the second video processing pipeline the second image decoded frame;

transmitting the processed first decoded frame into a first portion of a video buffer for updating the display with the processed first decoded frame;

storing the second processed decoded frame into a second portion of the video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Reynolds discloses receiving a first video data from a first video source at a first video decoder via a first video channel (see Fig. 1);

receiving a second video data from a second video source at a second video decoder via a second video channel (see Fig. 1);

decoding, via the first video decoder, a first frame of the first video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2);

decoding, via the second video decoder, a second frame of the second video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2);

inputting the first decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2, the decoded video signals/frames of Reynolds corresponding to the image inputs of Machida, see Machida, Fig. 3); and

inputting the second decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Reynolds, Fig. 2, the decoded video signals/frames of Reynolds corresponding to the image inputs of Machida, see Machida, Fig. 3).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Machida's system to include the limitations as taught by Reynolds for the same advantage as stated above regarding claim 1.

Machida in view of Reynolds does not specifically disclose transmitting the frame into a first portion of a video buffer for updating the display with the processed first decoded frame;

storing the second frame into a second portion of the video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Reitmeier discloses transmitting a first frame to a video buffer of a video buffer for updating the display with the processed first decoded frame (see Reitmeier, Fig. 1 and col 3, lines 66-67 and col 4, lines 63-65).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds to include the limitations as disclosed by Reitmeier for the advantage of providing a more efficient system for rapidly acquiring channels.

Machida in view of Reynolds and Reitmeier does not specifically disclose transmitting a first frame into a first portion of a video buffer,

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display, or

providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Miyazaki discloses transmitting a first frame into a first portion of a video buffer (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14), and

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Reitmeier to include the limitations as disclosed by Miyazaki for the advantage of reducing the latency of acquiring channels.

Machida in view of Reynolds, Reitmeier and Miyazaki does not specifically disclose providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines.

In an analogous art, Mizutome discloses providing a user option to select one of the first and second decoded frames for viewing in a particular view window of the display device via a manual I/O interface that is in operable communication with the first and second video processing pipelines (see Figs. 4 and 20 and related text).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds, Reitmeier and Miyazaki to include the limitations as taught by Mizutome for the advantage of providing an improved system capable of combining multiple video signals at a user location to effectively display multiple images in an output mode preferred by a user.

7. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record), Reitmeier (of record), Miyazaki (of record) and Mizutome (previously cited), as applied to claim 14 above, and further in view of Miura (of record).

Regarding claim 15, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome discloses processing, by a first video processing pipeline, a decoded first frame, but does not specifically disclose determining whether a first video source coupled to the first video processing pipeline is in a failed state.

In an analogous art, Miura discloses determining whether a first video source coupled to the first video processing pipeline is in a failed state (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome to include the limitations as disclosed by Miura for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 16, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses processing, by a first video processing pipelines, a first decoded frame comprising outputting a blacked out frame for a first video source upon determining that the first video source is in a failed state (see Miura, col 20, lines 49-54).

Regarding claim 17, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses switching a configuration of a second portion of a video buffer that is not updating a display with a part of a video buffer that is updating the display, upon determining that the first and second video processing pipelines have completed processing the first and second decoded frames (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 18, Machida in view of Reynolds, Reitmeier, Miyazaki and Mizutome, and further in view of Miura discloses scaling first and second decoded frames (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7) based on image size and the number of video sources (the number of video sources that are actually to be displayed, see Machida, col 5, lines 32-48).

8. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 19 above, and further in view of Miura (of record).

Regarding claim 23, Machida in view of Reynolds and Mizutome discloses a video processing pipeline, but does not specifically disclose executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time.

In an analogous art, Miura discloses executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 24, Machida in view of Reynolds and Mizutome, and further in view of Miura discloses a video fail operation comprising an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the plurality of video sources (see Miura, col 20, lines 49-54).

Regarding claim 25, Machida in view of Reynolds and Mizutome, and further in view of Miura discloses a video fail operation comprising an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure (see Miura, col 20, lines 49-54 and col 36, lines 20-33).

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Reynolds (of record) and Mizutome (previously cited), as applied to claim 19 above, and further in view of Kovacevic (of record).

Regarding claim 26, Machida in view of Reynolds and Mizutome does not specifically disclose analog video data.

In an analogous art, Kovacevic discloses analog video data (see [0026], lines 8-11).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Reynolds and Mizutome to include the limitations as taught by Kovacevic for the advantage of providing an improved system for displaying multiple images that allows for multiple types of video signals to be received, processed and viewed.

(10) Response to Argument

Note: ** This Supplemental Examiner's answer is to correct and clarify a typographical error made in the initial Examiner's answer mailed on 11/10/2010. In section (10) Response to Argument of the previous Examiner's Answer, at line 11, and at line 31, the Examiner made a typographical error in reciting "video signals 210 and 241 (see Reynolds, Fig. 2)". The correct recitation should have been "video signals 210 and 214 (see Reynolds, Fig. 2)", as further evidenced by the subsequent recitation "This, then, reasonably reads on the limitation of "video channels", as claimed. Furthermore, since Reynolds discloses that the video signal 210 is connected to video decoder 220, and video signal 214 is connected to video decoder 228, Reynolds does reasonably teach a video decoder being coupled to a different video channel, as claimed" at lines 11-15.

In response to the Appellant's arguments regarding the rejection of claim 1, specifically on page 10, lines 23-26 that, "However, Applicant respectfully submits that Reynolds" fails to

describe the subject matter ascribed to it by the Examiner when interpreted in light of the Applicant's specification. For example, Reynolds" fails to describe that "each video decoder [is] coupled to a different one of the plurality of video channels", and on page 11, lines 12-14 that, "Reynolds does NOT describe "a plurality of video decoders coupled to the plurality of video channels, **each [i.e., all] video decoder [is] coupled to a different one of a plurality of video channels**" the Examiner respectfully disagrees. Reynolds discloses at [0026], lines 1-11 that the video sources of his system may be of a cable television network, a satellite television network, etc. Reynolds further teaches that the multiple video feed signal 210, from the video sources, may be comprised of video signals 210 and 214 (see Reynolds, Fig. 2). This, then, reasonably reads on the limitation of "video channels", as claimed. Furthermore, since Reynolds discloses that the video signal 210 is connected to video decoder 220, and video signal 214 is connected to video decoder 228, Reynolds does reasonably teach a video decoder being coupled to a different video channel, as claimed.

In response to Appellant's arguments on page 12, lines 1-13 that, "Applicant respectfully submits that the Examiner's asserted definition of "channel" is improper and respectfully points out that the claims must be given their broadest reasonable interpretation, but this interpretation must be consistent with the specification (MPEP 2111) and that an Applicant may be his own lexicographer (MPEP 2111.01). In this respect, Applicant respectfully points to paragraph [0003] of the specification where it is expressly disclosed that "[a] typical synchronized 'n' channel analog video rendering system (displaying 'n' video channels simultaneously) displays the video at...the National Television Standards Committee (NTSC) analog video format standard." (emphasis added). Throughout the specification, it is a video or television channel

that is being discussed under the NTSC standard and not a physical signal path for transmitting signals under the particular IEEE standard asserted by the Examiner. Thus, the Applicant's express definition of "channel" is a television channel (i.e. an electronic signal) under the NTSC standard must prevail", the Examiner respectfully disagrees. Reynolds discloses at [0026], lines 1-11 that the video sources of his system may be of a cable television network, a satellite television network, etc. Reynolds further teaches that the multiple video feed signal 210, from the video sources, may be comprised of video signals 210 and 214 (see Reynolds, Fig. 2). This, then, reasonably reads on the limitation of "video channels", as claimed.

In response to Appellant's arguments on page 13, lines 18-24 that, "In her final rejection, the Examiner **concedes** that Machida fails to describe inputting the first and second decoded frames into a first and second video processing pipeline via **a non-blocking switch** (OA page 13, lines 14-*17). The Examiner then asserts that reyolds describes "inputting the first decoded frame" and "inputting the second decoded frame" but while doing so implicitly concedes that* Reynolds also fails to describe a non-blocking switch by omitting any assertion to the contray", the Examiner respectfully disagrees. The final ofiice action at page 13, lines 1-5 specifically sets forth Machida inputting a first and second image into a first and second video processing pipeline via a non-blocking switch (image selection means 101, see Machida, Fig. 3). Reynolds is specfically referenced to teach the corresponding elements of his system to Machida's.

In response to Appellant's arguments on page 14, lines 13-30 that, "Further, a prima facie case of obviousness cannot be established due to a lack of motivation to combine Machida with any of the other references because Machida teaches away from the claim elements (MPEP 2145 (X)(D)). This is so because Machida teaches away from the use of a non-blocking switch

(See, paragraph 0033 (image selection means 101 selects and outputs a prescribed number of images among the input images having high priority orders)). Passing along images in order of priority is antithetical to a non-blocking switch because each image cannot be processed/displayed concurrently without hindrance.

Machida expressly describes that images may only enter a processing channel 102 based on their priority assignment, which by definition entails a blocking mechanism and is contrary to a non-blocking switch. Therefore, there is no motivation to combine Machida with any of Reynolds, Reitmeier, Reitmeier, Miyazaki and Mizutome with a reasonable chance of success because Machida teaches the use of a blocking switch arrangement that relies on image priority as discussed above. As such, independent claim 14 is allowable over the current combination of references for at least this additional and independent reason. Claims 15-18 properly depend from independent claim 14 and are allowable therewith", and page 15, lines 6-16 that, "Further, even assuming that the Examiner's speculation is correct for the sake of this argument only, Applicant respectfully submits that the image selection means 101 of Machida is still a blocking switch mechanism regardless of whether or not on some speculative occasions the volume of images input may be equal to the available image processing channel 102. The Examiner's speculation is akin to arguing that that a reference describing a transistor is actually describing a short because on some occasions the transistor is biased to conduct a current. Just because the transistor is biased to conduct current from time to time, it does not follow that the reference is teaching a short circuit and not a transistor. Therefore, even if the Examiner's speculation about Machida is correct, the image selection means 101 is still a blocking switch and teaches away *from the claim recitations",* the Examiner respectfully disagrees. Machida's system discloses

that a priority order is given to the input images by the screen control means, and that the number of images to be output is determined by the screen control means 106. This number, may reasonably be all of the images input. As shown by Machida in Fig. 3, all of the output images are processed by an image processing means , without regard to order or dedication to a particular image processing means. Therefore, in this particular embodiment of Machida, the image selection means is a non-blocking switch. "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." In re Heck, 699 F.2d 1331, 1332-33, 216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting In re Lemelson, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). See also > Upsher-Smith Labs. v. Pamlab, LLC, 412 F.3d 1319, 1323, 75 USPQ2d 1213, 1215 (Fed. Cir. 2005)(reference disclosing optional inclusion of a particular component teaches compositions that both do and do not contain that component);< Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998) (The court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed.").

In response to Appellant's arguments on pages 15 - 16, section C, that, "Dependent claim 25 stands rejected under 35 U.S.C. § 103(a) as being obvious over Machida in view of Reynolds',

Mizutome and Miura. The Examiner rejects claim 25 by asserting that the combination of Machida and Reynolds" describes most of the claim elements but concedes that the combination fails to describe that "the video fail operation comprises an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure." The Examiner proceeds in her rejection by asserting that Miura cures the conceded discrepancy and cites Column 20; lines 49-54 and Column 36; lines 20-33 in support.

10. However, Applicant respectfully points out that Miura fails to describe the subject matter ascribed to Miura by the Examiner. Miura merely describes using a stored bit map such as a logo with an alphanumeric message (See, Col. 20; lines 49-55). A fixed bit map in memory cannot reasonably be construed to be an output of a previous image for the one of the plurality of video channels because the output of a previous image is ever changing and is determined only by the subject matter being displayed and the timing just prior to the failure. In other words, the previous image is a random image and not a stored static image that is specific to this purpose as is described in Miura", the Examiner respectfully disagrees. In addition to col 20, lines 49-54 and col 36, lines 20-33, the Appellant should please note that Miura discloses that in the event of a failure, a previous image (see col 21, lines 51-60 and Fig. 2C) is displayed, and that this process may be combined (see col 39, lines 15-16) with the step of including a type of special data in the event of a failure, such as a message of no input, etc. (see col 20, lines 46-53).

11. In response to Appellant's arguments on pages 16-17, section D, that, "For example, the Examiner has stipulated that the Reynolds processes that allegedly reading on the Applicant's base claims all take place in the interactive set top boxes (112/118), which process strictly digital data. As can be seen form Figure 1 of Reynolds, all analog data is converted to digital

data prior to being transmitted by Digital Video Distribution Network 104. Therefore, no processes occurring in the User's Locations 111 are capable of processing analog data. As such, a prima facie case of obviousness cannot be established because there is no motivation to modify Reynolds" (digital processing) by Kovacevic (using analog data) because there is no reasonable chance of success in processing analog data by digital circuitry (See, MPEP §2143.02) in processing the analog data of Kovacevic by the digital circuitry of Reynolds/Machida)", and "Similarly, the Examiner has also stipulated that the Machida processes that allegedly read on the Applicant's base claims all occur in the image selection means 100, which processes strictly digital data. As can be seen form FIG. 4 of Machida, all video analog data is converted to digital data at A/D converter 213, prior to being transmitted to the digital image selection means 100. Therefore, no processes occurring in the image selection means are capable of processing analog data. As such, a prima facie case of obviousness cannot be established because there is no motivation to modify Machida (digital processing) by Kovacevic (using analog data) because there is no reasonable chance of success in processing analog data by digital circuitry (See, MPEP §2143.02)", the Examiner respectfully disagrees. A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including non-preferred embodiments (see MPEP 2123). While Reynolds may disclose a digital distribution network, he also discloses that his "distribution network 104 may comprise a cable television network, satellite television network, internet video distribution network, or any other network capable of distributing video data" (see [0027], lines 4-8), which then must include any modifications and variations in light of his teachings (see Reynolds, [0061], lines 1-6), and thereby provides a reasonable motivation to modify his system in view of Kovacevic.

Furthermore, Fig. 3 of Machida, which does not show a processing of strictly digital data, and not Figure 4, was used to meet the limitations of the claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the reasons above, it is believed that the rejections should be sustained.

Respectfully submitted,

/CHENEA P SMITH/

Examiner, Art Unit 2421

/Christopher Kelley/

Supervisory Patent Examiner, Art Unit 2424

/FARZANA HOSSAIN/

Primary Examiner, Art Unit 2424